WHAT IS CLAIMED IS:

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1. A semiconductor memory integrated circuit comprising:

a semiconductor substrate;

a device isolation insulating film buried in grooves formed into said semiconductor substrate;

a cell array having an arrangement of electrically erasable and programmable nonvolatile memory cells made by stacking floating gates and control gates on said semiconductor substrate; and

a peripheral circuit disposed around said cell array on said semiconductor substrate,

at least the bottom layer of said floating gates of said nonvolatile memory cells and at least the bottom layer of gate electrodes of transistors in said peripheral circuit being formed before said device isolation insulating film is buried, then being maintained in self alignment with said device isolation insulating film, and impurities being doped thereto under different conditions from each other.

2. The semiconductor memory integrated circuit according to claim 1 wherein said transistors in said peripheral circuit have at least two gate insulating films different in thickness.

3. The semiconductor memory integrated circuit according to claim 1,

- wherein different n-type impurities are doped into said floating gates of said nonvolatile memory cells and gate electrodes of NMOS transistors in said peripheral circuit, and a p-type impurity is doped into said gate electrodes of PMOS transistors in said peripheral circuit.

4. The semiconductor memory integrated circuit according to claim 1,

- wherein phosphorus is doped into said floating gates of said nonvolatile memory cells.

5. The semiconductor memory integrated circuit according to claim 1,

wherein phosphorus is doped into said floating gates of said nonvolatile memory cells, and arsenic is doped into said gate electrodes of NMOS transistors in said peripheral circuit.

6. The semiconductor memory integrated circuit according to claim 1 wherein said floating gates of said nonvolatile memory cells comprise of a first-layer gate electrode material film in self alignment with said device isolation insulating film and a second-layer gate electrode material film stacked on said first gate electrode material film, said control gates comprise of a third-layer electrode material film, and said gate electrodes in said peripheral circuit have a three-layered structure including said first- to third-layer gate electrode material films.

7. The semiconductor memory integrated circuit according to claim 1 wherein said floating gates of said nonvolatile memory cells comprise of a first-layer gate electrode material layer in self alignment with said device isolation insulating film and a second-layer gate electrode material film, said gate electrodes comprise of a third-layer gate electrode material film, and said gate electrodes in said peripheral circuit have a two-layered structure including said first- and third-layer gate electrode material films.

8. The semiconductor memory integrated circuit according to claim 1 wherein said floating gates of said nonvolatile memory cells comprise of a first-layer gate electrode material layer in self alignment with said device isolation insulating film and a second-layer gate electrode material film, and said gate electrodes in said peripheral circuit also have a two-layered film structure including said first- and second-layer gate electrode material films.

9. A method of manufacturing a semiconductor memory

integrated circuit comprising:

forming a plurality of gate insulating films each having a thickness required for each of a cell array region and a peripheral circuit region on a semiconductor substrate;

forming a first-layer gate electrode material film not doped with impurities on said gate insulating films;

etching said semiconductor substrate covered with said first-layer gate electrode material film to make grooves for device isolation, and burying the device isolation grooves with a device isolation insulating film;

forming a second-layer gate electrode material film not doped with impurities on said first-layer gate electrode material film maintained in self alignment with regions surrounded by said device isolation insulating film and on said device isolation insulating film;

selectively introducing impurities into said first-layer and second-layer gate electrode material films in said cell array region;

selectively etching said second-layer gate electrode material film to isolate same on said device isolating insulating film in said cell array region;

forming a gate insulating film on said second-layer gate electrode material film to serve as an insulation film between floating gates and control gates of memory cells;

removing said gate insulating film from said peripheral circuit region;

forming a third-layer gate electrode material film not doped with impurities on said gate insulating film;

processing the gate electrode material in said memory cell region and said peripheral circuit region into a desired pattern to form control gate and floating gates in said memory cell region and form gate electrodes in said peripheral circuit region; and

forming source and drain diffusion layers and lowering the resistance of said gate electrodes by introducing impurities into said memory cell region and said peripheral circuit region under a plurality of different conditions.

10. The method of manufacturing a semiconductor memory integrated circuit according to claim 9 wherein the step of selectively introducing impurities into said first-layer and second-layer gate electrode material films is ion-implantation of phosphorus.

11. The method of manufacturing a semiconductor memory integrated circuit according to claim 9 wherein the step of forming source and drain diffusion layers and lowering the resistance of said gate electrodes includes ion implantation of arsenic into said cell array region and NMOS transistor regions in said peripheral circuit region, and ion implantation of boron into PMOS transistor regions in said peripheral circuit region.

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12. A method of manufacturing a semiconductor memory integrated circuit comprising:

forming a plurality of gate insulating films each having a thickness required for each of a cell array region and a peripheral circuit region on a semiconductor substrate;

forming a first-layer gate electrode material film not doped with impurities on said gate insulating films;

etching said semiconductor substrate covered with said first-layer gate electrode material film to make grooves for device isolation, and burying the device isolation grooves with a device isolation insulating film;

forming a second-layer gate electrode material film not doped with impurities on said first-layer gate electrode material film maintained in self alignment with regions surrounded by said device isolation insulating film and on said device isolation insulating film;

selectively introducing impurities into said first-layer and second-layer gate electrode material films in said cell array region;

selectively etching said second-layer gate electrode material film to isolate same on said device isolating insulating film in said cell array region;

forming a gate insulating film on said second-layer gate

electrode material film to serve as an insulation film between floating gates and control gates of memory cells;

forming a third-layer gate electrode material film on said gate insulating film;

removing said third-layer gate electrode material film from said peripheral circuit region;

processing the gate electrode material in said memory cell region and said peripheral circuit region into a desired pattern to form control gates and floating gates in said memory cell region and form gate electrodes in said peripheral circuit region; and

forming source and drain diffusion layers and lowering the resistance of said gate electrodes by introducing impurities into said memory cell region and said peripheral circuit region under a plurality of different conditions.

13. The method of manufacturing a semiconductor memory integrated circuit according to claim 12 wherein the step of selectively introducing impurities into said first-layer and second-layer gate electrode material films is ion-implantation of phosphorus.

14. The method of manufacturing a semiconductor memory integrated circuit according to claim 12 wherein the step of forming source and drain diffusion layers and lowering the resistance of said gate electrodes includes ion implantation of arsenic into said cell array region and NMOS transistor regions in said peripheral circuit region, and ion implantation of boron into PMOS transistor regions in said peripheral circuit region.

15. A method of manufacturing a semiconductor memory integrated circuit comprising:

forming a plurality of gate insulating films each having a thickness required for each of a cell array region and a peripheral circuit region on a semiconductor substrate;

forming a first-layer gate electrode material film not doped with impurities on said gate insulating films;

selectively etching said semiconductor substrate covered

with said first-layer gate electrode material film to form device isolation grooves, and burying said device isolation grooves with a device isolation insulating film;

forming a barrier film on said device isolation insulating film and said first-layer gate electrode material film maintained in self-alignment in regions surrounded by said device isolation insulating film to prevent diffusion of impurities;

selectively removing said barrier film from above said cell array region;

forming on the entire surface a second-layer gate electrode material film doped with impurity;

selectively etching said second-layer gate electrode material film to remove said second-layer gate electrode material film from above said device isolation insulation film within said cell array region, and removing said second-layer gate electrode material film from said peripheral circuit region;

forming a third-layer gate electrode material film not doped with impurities on said cell array region having said gate insulating film selectively formed on said second-layer gate electrode material film and on said peripheral circuit region from which said barrier film has been removed;

selectively etching said first-layer and third-layer gate electrode material films to form control gates and floating gates in said cell array region and gate electrodes in said peripheral circuit region; and

forming source and drain diffusion layers and lowering the resistance of said gate electrodes by introducing impurities into said memory cell region and said peripheral circuit region under a plurality of different conditions.

16. The method of manufacturing a semiconductor memory integrated circuit according to claim 15 wherein the impurity doped into said second-layer gate insulating film is phosphorus.

17. The method of manufacturing a semiconductor memory integrated circuit according to claim 15 wherein the step of forming source and drain diffusion layers and lowering the

resistance of said gate electrodes includes ion implantation of arsenic into said cell array region and NMOS transistor regions in said peripheral circuit region, and ion implantation of boron into PMOS transistor regions in said peripheral circuit region.

18. The method of manufacturing a semiconductor memory integrated circuit according to claim 15 wherein said barrier film is a silicon oxide film or a silicon nitride film.

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19. A method of manufacturing a semiconductor memory integrated circuit comprising:

forming a plurality of gate insulating films each having a thickness required for each of a cell array region and a peripheral circuit region on a semiconductor substrate;

forming a first-layer gate electrode material film not doped with impurities on said gate insulating films;

selectively etching said semiconductor substrate covered with said first-layer gate electrode material film to form device isolation grooves, and burying said device isolation grooves with a device isolation insulating film;

doping an impurity into said first-layer gate electrode material film on said cell array region;

etching the entire surface of said device isolation insulating film projecting upward to a level exposing side surfaces of said first-layer gate electrode material film;

forming a gate insulating film to cover said first-layer gate electrode material film;

forming a second-layer gate electrode material film over the entire surface;

selectively etching said first-layer and second-layer gate electrode material films to form control gates and floating gates in said cell array region and gate electrodes in said peripheral circuit region; and

forming source and drain diffusion layers and lowering the resistance of said gate electrodes by introducing impurities into said cell array region and said peripheral circuit region under a plurality of different conditions.

20. A method of manufacturing a semiconductor memory integrated circuit comprising:

forming a plurality of gate insulating films each having a thickness required for each of a cell array region and a peripheral circuit region on a semiconductor substrate;

forming a first-layer gate electrode material film not doped with impurities on said gate insulating films;

selectively etching said semiconductor substrate covered with said first-layer gate electrode material film to form device isolation grooves, and burying said device isolation grooves with a device isolation insulating film;

forming a barrier film on said device isolation insulating film and said first-layer gate electrode material film maintained in self-alignment in regions surrounded by said device isolation insulating film to prevent diffusion of impurities;

selectively removing said barrier film from above said cell array region;

forming on the entire surface a second-layer gate electrode material film doped with impurity;

removing the entire surface of said second-layer gate electrode material film to the level of and exposing the top surface of said device isolation insulating film in said cell array region;

removing said second-layer gate electrode material film from said peripheral circuit region;

etching the entire surface of said device isolation insulating film projecting upward to a level exposing side surfaces of said first-layer gate electrode material film;

forming a gate insulating film to cover said second-layer gate electrode material film on said cell array region;

forming a third-layer gate electrode material film on the entire surface;

selectively etching said first-layer to third-layer gate electrode material films to form control gates and floating gates in said cell array region and gate electrodes in said peripheral circuit region; and

forming source and drain diffusion layers and lowering the resistance of said gate electrodes by introducing impurities into said cell array region and said peripheral circuit region under a plurality of different conditions.